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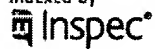
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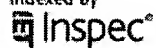
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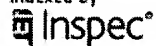
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### Compiled HW/SW co-simulation

1

Vojin Živojnovic, Heinrich Meyr

June 1996 **Proceedings of the 33rd annual conference on Design automation**

**Publisher:** ACM Press

Full text available: pdf(217.66 KB)

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1 [RASSP virtual prototyping of DSP systems](#)



C. Hein, J. Pridgen, W. Kline

June 1997 **Proceedings of the 34th annual conference on Design automation DAC '97**

**Publisher:** ACM Press

Full text available: pdf(128.85 KB)



[Publisher Site](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper describes a top-down hierarchical simulation process that dramatically accelerates the design-evolution of DSP systems when compared with traditional physical prototyping methods. A summary of the model abstraction hierarchy and purposes for the various types of models provides critical guidance in selecting appropriate abstractions to achieve accurate yet efficient simulations. The simulations enable rapid exploration of many more alternative software and hardware solutions than would be ...

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### 1 [Application specific architecture design tools: Performance simulation modeling for](#)



#### [fast evaluation of pipelined scalar processor by evaluation reuse](#)

Ho Young Kim, Tag Gon Kim

 June 2005 **Proceedings of the 42nd annual conference on Design automation**

Publisher: ACM Press

 Full text available: pdf(834.72 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper proposes a rapid and accurate evaluation scheme for cycle counts of a pipelined processor using evaluation reuse technique. Since exploration of an optimal processor is a time-consuming task due to large design space, fast evaluation methodology for an architecture is crucial. We introduce the performance simulation model which can evaluate the performance without considering the functional correctness. This model has an FSM-like form and can afford to take all hazard types of pipelin ...

**Keywords:** compiled simulation, evaluation reuse, instruction set architecture, retargetable simulation, trace-driven simulation

### 2 [Statistical sampling of microarchitecture simulation](#)



Roland E. Wunderlich, Thomas F. Wenisch, Babak Falsafi, James C. Hoe

 July 2006 **ACM Transactions on Modeling and Computer Simulation (TOMACS)**, Volume 16 Issue 3

Publisher: ACM Press

 Full text available: pdf(667.80 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Current software-based microarchitecture simulators are many orders of magnitude slower than the hardware they simulate. Hence, most microarchitecture design studies draw their conclusions from drastically truncated benchmark simulations that are often inaccurate and misleading. This article presents the Sampling Microarchitecture Simulation (SMARTS) framework as an approach to enable fast and accurate performance measurements of full-length benchmarks. SMARTS accelerates simulation by selective ...

**Keywords:** Microarchitecture simulation, SPEC CPU2000 simulation, cold-start bias, simulation sampling, statistical sampling

3

### [A hardware/software co-design flow and IP library based on simulink](#)



L. M. Reyneri, F. Cucinotta, A. Serra, L. Lavagno

June 2001 **Proceedings of the 38th conference on Design automation**

**Publisher:** ACM Press

Full text available: pdf(119.94 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This paper describes a design flow for data-dominated embedded systems. We use The Mathworks' Simulink\trademark environment for functional specification and algorithmic analysis. We developed a library of Simulink blocks, each parameterized by design choices such as implementation (software, analog or digital hardware, \ldots) and numerical accuracy (resolution, S/N ratio). Each block is equipped with empirical models for cost (code size, chip area) and performance (timing, energy), based ...

#### 4 Control Flow Modeling in Statistical Simulation for Accurate and Efficient Processor



##### Design Studies

Lieven Eeckhout, Robert H. Bell Jr., Bastiaan Stougie, Koen De Bosschere, Lizy K. John  
March 2004 **ACM SIGARCH Computer Architecture News , Proceedings of the 31st annual international symposium on Computer architecture ISCA '04**,  
Volume 32 Issue 2

**Publisher:** IEEE Computer Society, ACM Press

Full text available: pdf(228.94 KB)

Additional Information: [full citation](#), [abstract](#)

Designing a new microprocessor is extremely time-consuming. One of the contributing reasons is that computer designers rely heavily on detailed architectural simulations, which are very time-consuming. Recent work has focused on statistical simulation to address this issue. The basic idea of statistical simulation is to measure characteristics during program execution, generate a synthetic trace with those characteristics and then simulate the synthetic trace. The statistically generated synthetic trace ...

#### 5 System-level power estimation and optimization: A power estimation methodology for systemC transaction level models



Nagu Dhanwada, Ing-Chao Lin, Vijay Narayanan

September 2005 **Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis CODES+ISSS '05**

**Publisher:** ACM Press

Full text available: pdf(266.54 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Majority of existing works on system level power estimation have focused on the processor, while there are very few that address power consumption of peripherals in a SoC. With the presence of complex cores in current day embedded system-on-chip devices, the problem of complete system level power estimation is gaining significance. Transaction level models for SoCs are gaining increasing attention with emerging architectural modeling standards like SystemC. In this paper we present a methodology ...

**Keywords:** CoreConnect, PowerPC, power analysis, systemC, transaction level models

#### 6 Advances in hardware/software co-simulation techniques: RTOS-centric hardware/software cosimulator for embedded system design



Shinya Honda, Takayuki Wakabayashi, Hiroyuki Tomiyama, Hiroaki Takada

September 2004 **Proceedings of the 2nd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis**

**Publisher:** ACM Press

Full text available: pdf(510.21 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents an RTOS-centric hardware/software cosimulator which we have

developed for embedded system design. One of the most remarkable features in our cosimulator is that it has a complete simulation model of an RTOS which is widely used in industry, so that application tasks including RTOS service calls are natively executed on a host computer. Our cosimulator also features cosimulation with functional simulation models of hardware written in C/C++ and cosimulation with HDL simulators ...

**Keywords:** RTOS, cosimulation, embedded Systems

## 7 Performance evaluation of the PowerPC 620 microarchitecture



Trung A. Diep, Christopher Nelson, John Paul Shen

May 1995 **ACM SIGARCH Computer Architecture News , Proceedings of the 22nd annual international symposium on Computer architecture ISCA '95**, Volume 23 Issue 2

**Publisher:** ACM Press

Full text available: pdf(1.35 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citings](#), [index terms](#)

The PowerPC 620 microprocessor is the most recent and performance leading member of the PowerPC family. The 64-bit PowerPC 620 microprocessor employs a two-phase branch prediction scheme, dynamic renaming for all the register files, distributed multi-entry reservation stations, true out-of-order execution by six execution units, and a completion buffer for ensuring precise exceptions. This paper presents an instruction-level performance evaluation of the 620 microarchitecture ...

## 8 Design Space Exploration for a Wireless Protocol on a Reconfigurable Platform

Laura Vanzago, Bishnupriya Bhattacharya, Joel Cambonie, Luciano Lavagno

March 2003 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1 DATE '03**

**Publisher:** IEEE Computer Society

Full text available: pdf(175.69 KB)

Additional Information: [full citation](#), [abstract](#), [index terms](#)



[Publisher Site](#)

This paper describes a design space exploration experiment for a real application from the embedded networking domain at the physical layer of a wireless protocol. The application models both control oriented as well as data processing functions, and hence require composing tasks from different models of computation. We show how the cost and performance of communication and computation can be quickly evaluated, with a reasonable modeling cost. While the example uses a specific tool, the methodology ...

## 9 Reactive Techniques for Controlling Software Speculation

Craig Zilles, Naveen Neelakantam

March 2005 **Proceedings of the international symposium on Code generation and optimization CGO '05**

**Publisher:** IEEE Computer Society

Full text available: pdf(327.69 KB)

Additional Information: [full citation](#), [abstract](#), [index terms](#)

Aggressive software speculation holds significant potential, because it enables program transformations to reduce the program's critical path. Like any form of speculation, however, the key to software speculation is employing it only where it is likely to succeed. While mechanisms for controlling hardware speculation (e.g., saturating counters updated after each instance) are well understood, these techniques do not translate directly to software techniques because changing a speculation requires ...

## 10 HW/SW codesign of an engine management system

M. Baleani, A. Ferrari, A. Sangiovanni-Vincentelli, C. Turchetti

January 2000 **Proceedings of the conference on Design, automation and test in**

**Europe****Publisher:** ACM Press

Full text available: pdf(89.22 KB)

[Publisher Site](#)Additional Information: [full citation](#), [references](#), [index terms](#)**11** Session 3: sampling: Improved automatic testcase synthesis for performance model validation 

Robert H. Bell, Lizy K. John

June 2005 **Proceedings of the 19th annual international conference on Supercomputing ICS '05****Publisher:** ACM Press

Full text available: pdf(1.41 MB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Performance simulation tools must be validated during the design process as functional models and early hardware are developed, so that designers can be sure of the performance of their designs as they implement changes. The current state-of-the-art is to use simple hand-coded bandwidth and latency testcases to assess early performance and to calibrate performance models. Applications and benchmark suites such as SPEC CPU are difficult to set up or take too long to execute on functional models. ...

**Keywords:** automatic benchmark synthesis, benchmarking, performance modeling, synthetic benchmarks

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